WHAT IS CLAIMED IS:

1. A method of controlling leakage current within an integrated circuit comprising the steps of:

determining whether a current carrying device within the integrated circuit is susceptible to exhibiting an unacceptable level of leakage current;

responsive to said determination, adjusting the threshold voltage of the current carrying device to reduce the current carrying capacity of the device if the device is susceptible to exhibiting an unacceptable amount of leakage current by adjusting the threshold voltage comprises the step of reducing the current carrying capability of a source resistance transistor connected in series with the current carrying device by connecting a control gate of the source resistance transistor to a predetermined voltage level if the threshold voltage of the current carrying device is to be adjusted; and

connecting the control gate of the current limiting device to a second predetermined voltage level to allow the current limiting device to conduct a full measure of current if the threshold voltage of the current carrying device is determined to remain unchanged by the source resistance transistor.

2. An electronic circuit comprising:

a source resistance transistor connected to a first supply voltage;

a current carrying transistor connected between the source resistance transistor and a second supply voltage; and

a control gate of the source resistance transistor connected to a bond pad that is electrically connectible to either the first or second supply voltages, the connection of the control gate of the source resistance transistor to the first supply voltage resulting in the reduction of the current carrying capacity of the source resistance transistor and a corresponding increase in

the threshold voltage of the current carrying transistor thereby reducing the leakage current through the current carrying transistor.

3. The circuit of Claim 2 wherein the control gate of the source resistance transistor is connected to the second supply voltage such that the source resistance transistor is able to conduct electricity at full capacity and the threshold voltage of the current carrying transistor is left substantially unchanged.

4. The circuit of Claim 2 wherein the connection of the control gate of the source resistance transistor is made by a conductive layer defined by photolithographic mask used during the creation of the circuit.

5. The circuit of Claim 2 wherein the connection of the control gate of the source resistance transistor is made by connecting bond pads respectively connected to the first supply voltage and to the control gate at the time the semiconductor die on which the circuit is disposed is bonded to a package frame.

6. The circuit of Claim 2 wherein the connection is made within a package in which the die on which the circuit is disposed is placed.

7. The circuit of Claim 2 wherein the control gate and the first and second supply voltages are each separately connected to a pin of a package containing the circuit and wherein the connection of control gate to either the first or second supply voltages are made by systems external to the package containing the circuit.

8. An electronic system comprising:

a first circuit comprising a current carrying device and a current limiting device connected in series between first and second supply voltages; and

a diagnostic circuit operable to determine whether the electronic system is operating at a sufficient operating current level, the diagnostic circuit operable to connect a control gate of the current limiting device to either the first or second supply voltage levels to change the threshold voltage of the current carrying device and thereby change the amount of current used by the current carrying device.

9. A method for adjusting the performance of an integrated circuit in accordance with device parameters and application requirements comprising the steps of:

determining a desired adjustment; and

connecting a control node of the integrated circuit to one of a plurality of supply voltages to adjust the operation of devices in the integrated circuit.

10. The method of Claim 9 wherein the step of determining the desired adjustment comprises the step of measuring the threshold voltage of an associated test transistor.

11. The method of Claim 9 wherein the step of determining the desired adjustment comprises the step of measuring the standby current of the integrated circuit.

12. The method of Claim 9 wherein the step of determining the desired adjustment comprises the step of comparing the performance of the integrated circuit to a specification for a selected application.

13. The method of Claim 9 wherein the control node is connected to the gate of a source resistance transistor.

14. The method of Claim 9 wherein the step of connecting a control node to one of a plurality of supply voltages is accomplished by selection of a metal interconnect pattern in the manufacture of the integrated circuit.

15. The method of Claim 9 wherein the step of connecting a control node to one of a plurality of supply voltages is accomplished by bonding.

16. The method of Claim 9 wherein the control node is connected to a chip input and the selected voltage is supplied by the system using the integrated circuit.

17. An integrated circuit comprising:

a control node selectively connected to a supply voltage; and

the voltage on said control node modifying the standby current of the integrated circuit.

18. An electric circuit comprising:

a source resistance transistor;

a switchable transistor associated with the source resistance transistor; and

a control gate of the source resistance transistor that is electrically connectable to one of a plurality of supply voltages, the connection of the control gate of the source resistance transistor to one of the plurality of supply voltages affecting the performance of the switchable transistor.

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